Nepal College of Information Technology

**Assessment**

Fall 2012

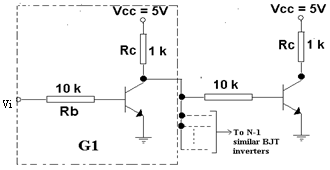
Program : CE/ELX Time : 3 hrs

Semester : Fall (V) FM : 100

Subject : Integrated Digital Electronics PM : 50

* *Candidates are requested to give their answer as far as practicable in their own words.*
* *The figure in the margin indicates the full marks*
* ***Attempt ALL question***

**1. a.**  Assuming  = 70, VBE (on) = 0.65 V, VBE (sat) = 0.75 V, .VCE (sat) = 0.2 V, calculate noise margins for fan-out(N)=10, for the BJT inverter G1 shown in the figure below. [7] ...**(7)**



**b.** With suitable circuit diagrams, explain how the speed of propagation can be improved in an ordinary RTL gate.

**Or**

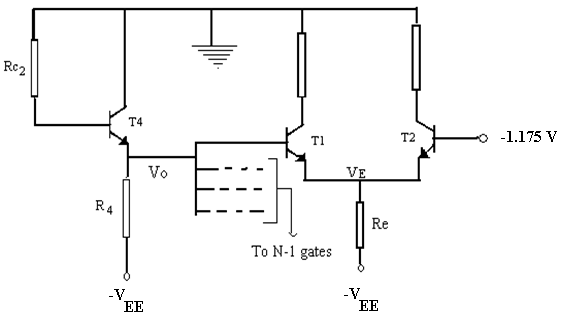
Explain the following terms:Charge Compensation and Active Pull-up. [8]

**2 a.** Derive the expression for the fan-out(N) for the IC DTL NAND gate.[8]

**Or**

Draw the two-input Discrete DTL NAND gate and explain its operation in detail.

**b.** The OR output of the ECL gate is shown below to be fanned out to N similar gates. Find N at room temperature if the ∆1 noise margin is to be 0.3. Assume that the resistors of driving stage are 20% higher than typical and the resistors of driven stages ...... are 20% lower than typical. The supply voltage is 10% higher and the transistor have .current gains, hFE = 40.The departures from the typical values are all in the direction … . .to reduce the fan-out.The typical values are RC2 = 300Ω, R4 =1500Ω, Re =1180Ω, and VEE =5.2 V. **(7)**



**3. a.** Draw the high speed TTL circuit and explain how the following factors account for the high speed in it. **(8)**

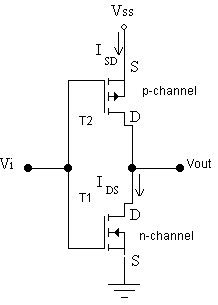
**OR**

Draw the tri-state TTL gate circuit and explain its working in detail.[8]

**b.** Draw the circuit diagram for the ECL gate and explain why ECL is faster than other BJT logic families. [7]

**4. a.** Define the following terms:Noise margins,Propagation speed,Fan-out,Power dissipation,Packing density and Temperature sensitivity. **(8)**

**b.** Consider the CMOS inverter given below. For Kn = Kp , VT (n) = VT (p) = 2V and VSS =10V, find the unique input voltage Vi(sat) defined by the simultaneous saturation of both ............transistors. **(4)**



**c.** The rise time in NMOS is extremely long in comparison to the fall time whereas in ....case of CMOS both are almost equal. Why? **(3)**

**5. a.** Draw the circuit and explain read, write and refresh operations in a four-transistor MOS dynamic cell **or** three-transistor MOS dynamic cell. **(8)**

6. a. Write the VHDL code for the behavioural description of a buzzer that gives a warning signal when the car key is inserted in an ignition lock when the door is open and seat belt is not used.

**OR**

Write the VHDL code for the structural description of a half adder. [7]

7. Write short notes on.***(Any two)***  [10]

a. IIL

b. RTL Exclusive OR gate

c. Analytic equations of MOSFETs

d. 2-input CMOS NAND gate.